1   *****

2

3   Therefore, methods and apparatus for implementing a Reprogrammable Instruction DSP,

4   have been described.

5

6   It should be understood that the particular embodiments described above are only

7   illustrative of the principles of the present invention, and various modifications could be

8   made by those skilled in the art without departing from the scope and spirit of the

9   invention. Thus, the scope of the present invention is limited only by the claims that

10   follow.

11   * * * * * *

12

13   Therefore, a methods and apparatus for implementing a combination video/voicemail

14   system especially useful in the construction industry and other industries requiring

15   remote viewing with guidance and supervision, has been described

16

17   It should be understood that the particular embodiments described above are only

18   illustrative of the principles of the present invention, and various modifications could be

19   made by those skilled in the art without departing from the scope and spirit of the

20   invention. Thus, the scope of the present invention is limited only by the claims that

21   follow.

22

23   **CLAIMS**

24

25   What is claimed is:

26

27   1.   A semiconductor device including a processor having reprogrammable

28   instructions implemented in field-programmable logic, where all I/O connections for said

29   field-programmable logic connect to said DSP processor.

30

1   2.   A family of two or more ASIC devices including a processor having mask-

2   programmable instructions implemented in ASIC logic, each device member of said

3   family having different amounts of ASIC logic available, and each member of said device

4   family having substantially identical processors, processor memory, and numbers of I/O.

5

6   3.   The device family of ASIC devices of claim 2 where all members of said family

7   can plug into the same socket in a target system and function properly.

8

9   4.   A method for implementing DSP software functionality in a device containing a

10   processor and field-programmable logic, comprising:

11   performance-profiling the execution of said DSP software functionality to identify

12   the subroutine that dominates the overall execution time ; and

13   automatically converting, by computer means, the subroutine that dominates the

14   overall execution time into field programmable logic functionality, such that the field

15   programmable logic implementation of said subroutine is implemented in synchronous

16   logic.

17

18   5.   The method of claim 4 where said the field programmable logic implementation

19   of said subroutine is implemented in logic that is synchronous with the clocks of said

20   DSP processor.

21

22   6.   The method of claim 4 where said dominant subroutine is implemented in mask-

23   programmed ASIC logic.

24

25   7.   A method for implementing DSP software functionality in a prototype device

26   containing a processor and field-programmable logic and a production device containing

27   mask-programmed ASIC logic functionality, comprising:

28   performance-profiling the execution of said DSP software functionality to identify

29   the subroutine that dominates the overall execution time; and

30   converting the subroutine that dominates the overall execution time into field-

31   programmable logic functionality; and

1   evaluating the device size and speed required for implementation in a production

2   device where the function implemented in said field-programmable logic functionality is

3   instead implemented using mask-programmed ASIC logic functionality.

4

5

6

"Reprogrammable Instruction DSP"
Robert Osann, Jr., 10494 Ann Arbor Ave., Cupertino, CA 95014, 408-313-1990, Bob@Osann.com